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ARCHITECTURE AND DESIGN CONSIDERATIONS OF A MASS MEMORY MODULE FOR SMALL SATELLITE PLATFORMS

Abstract

The increasing number of satellites, particularly for Earth observation such as Synthetic Aperture Radar (SAR), requires efficient on-board data processing solutions due to limited downlink capacity. The EU Horizon Europe project SOPHOS aims to develop high-performance processing technologies focused on SAR applications in small satellites. In this paper we present the design of a high-performance Mass Memory Module (MMM) for this application.

The SOPHOS system includes a Payload Processing Module (PPM), MMM, and Electronic Ground Support Equipment (EGSE) with a SAR instrument emulator and ground segment. The demonstrator uses 10Gb Ethernet for high rate payload data transfer and SpaceWire for command and control (CC).

Data can be stored in the MMM, processed in the PPM, or sent to ground, enabled by a routing function in the MMM for flexible data handling. For the PPM, Unibap's SpaceCloud system, cutting-edge commercial off-the-shelf (COTS) components are considered, enabling high-volume in-orbit data processing. In contrast, the MMM uses qualified, radiation-tolerant devices for reliable long-term storage, representing a mixed-criticality approach in the design. To demonstrate the performance of the system, advanced SAR image formation processing and raw data compression algorithms are developed and optimized for the PPM.

The MMM consists of three interconnected PCBs: Mass Memory Board (MMB), Interface and Processing Board (IPB), and Power Supply Board (PSB).

The MMB includes Flash memory for non-volatile data storage with a capacity of up to 50Tbit EOL, utilizing 24x 8 Tbit NAND Flash devices in SLC mode, allowing for high data rates up to 10 Gbit/s. The IPB is centered around a radiation-tolerant Microchip RT Polarfire FPGA and includes DDR4-SDRAM for data buffering. It features high-speed data interfaces (4x10Gb Ethernet with optical transceivers) and command and control interfaces (2xSpaceWire). The IPB's design is adaptable to various interfaces based on customer needs.

A soft-core LEON3FT CPU in the FPGA controls the MMM, running boot loader and application software for data management. The SpaceWire CC interface includes heritage SpaceWire IP with a switchable nominal and redundant interface. The MMM also incorporates EDAC functionality for error detection and correction in memory storage.

The PSB provides primary and secondary power conversion and overvoltage protection for the MMB and IPB. The three PCBs are stacked within dimensions of 132mm x 127 mm, achieved through high-density placement and routing and the average power consumption of the MMM is estimated at 20W, thus complying with the requirements for the application in small satellite platforms.